

FIG. 1A

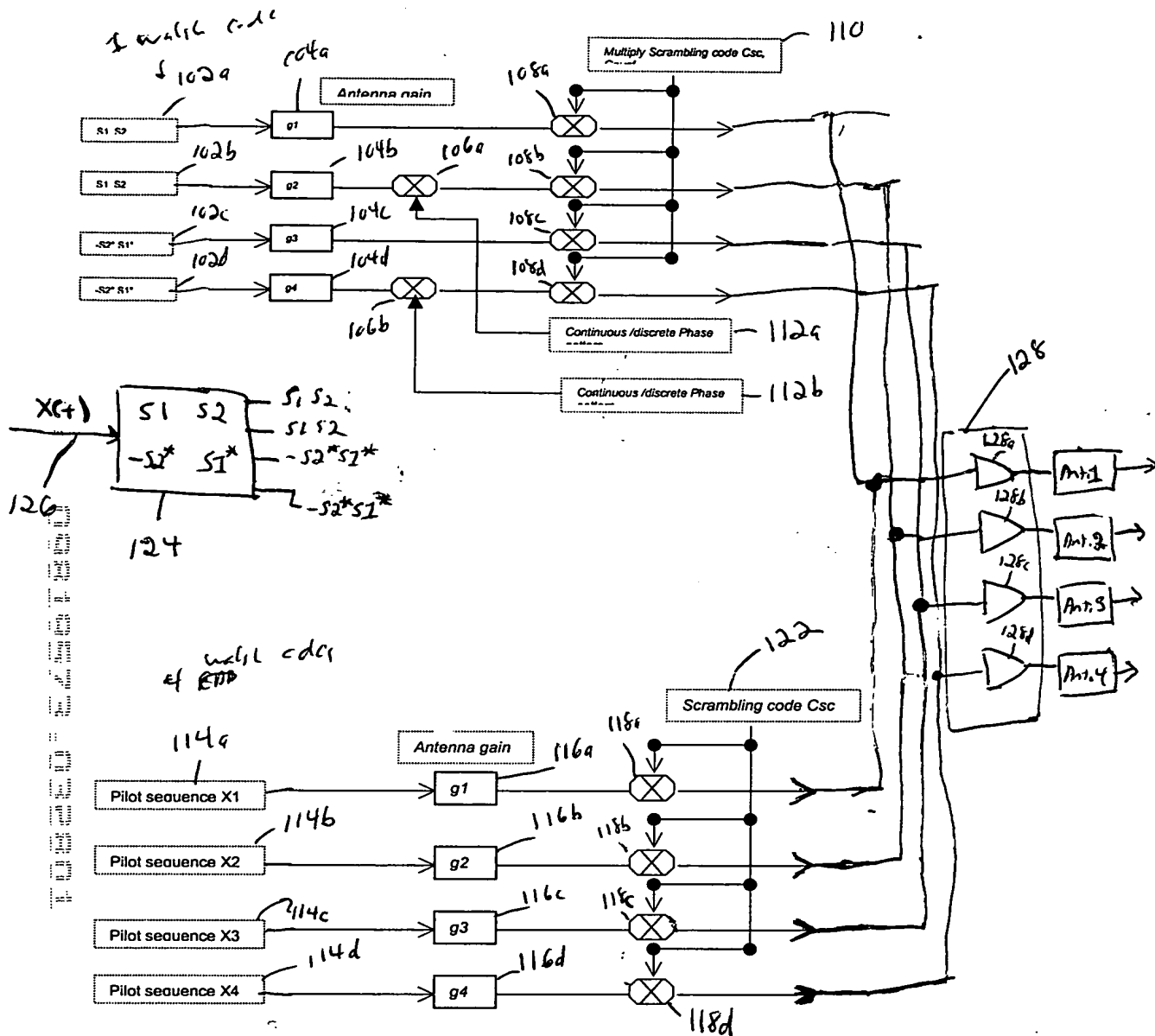


FIG. 1d

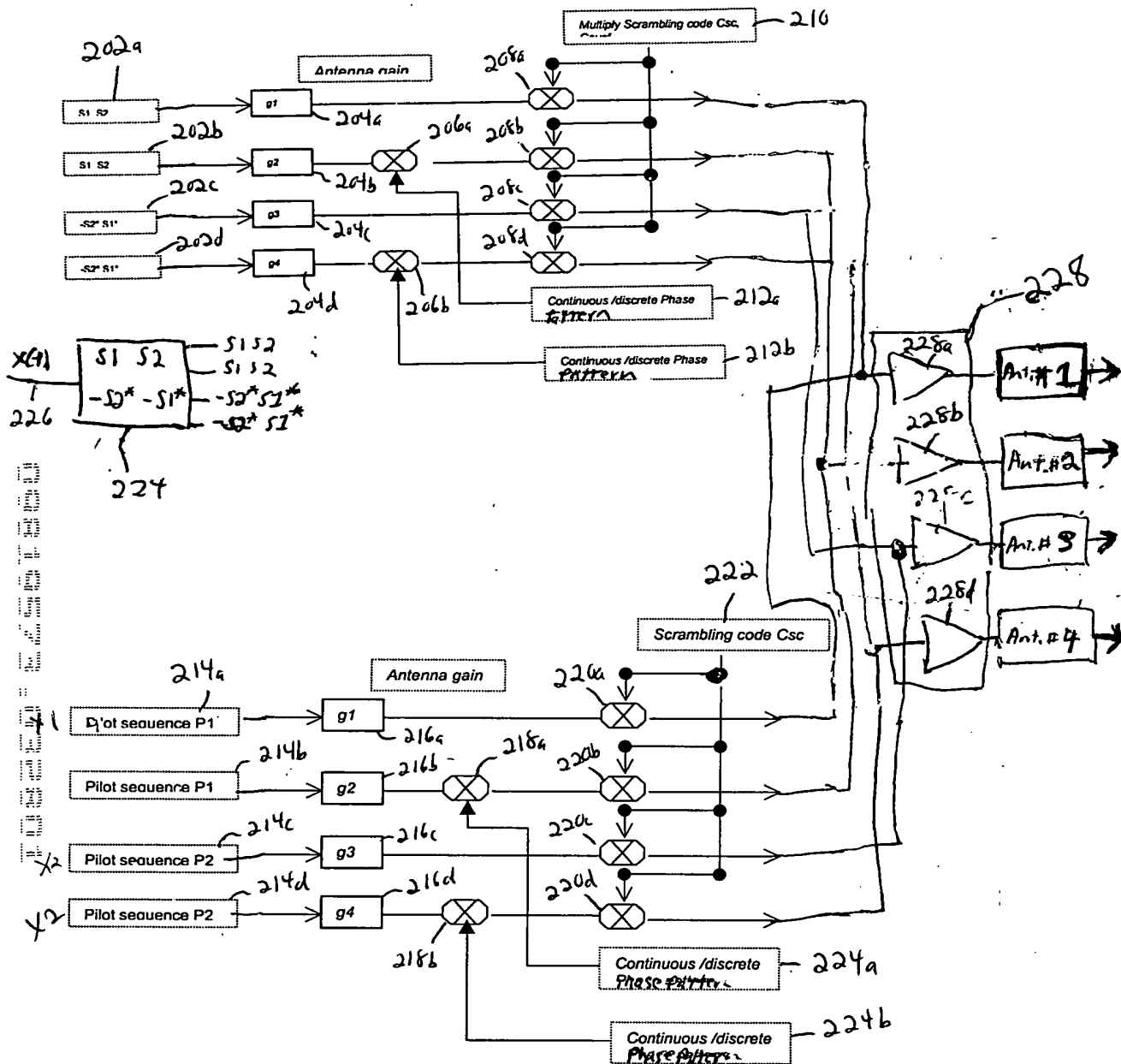


Fig. 2.

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300

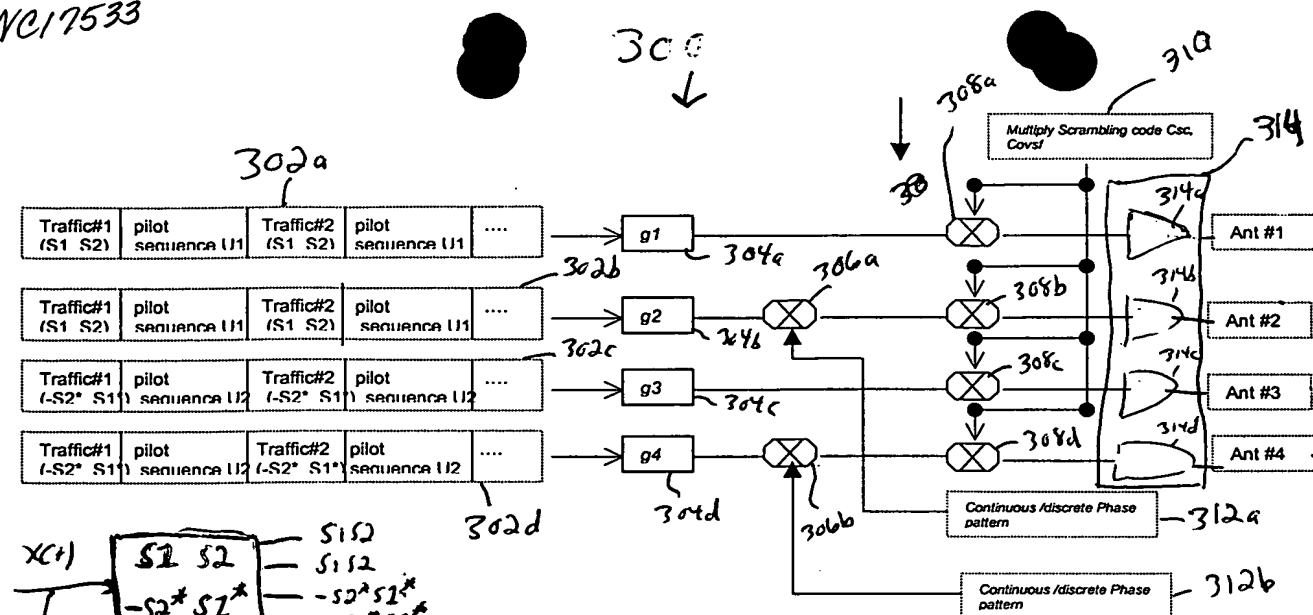


FIG. 3

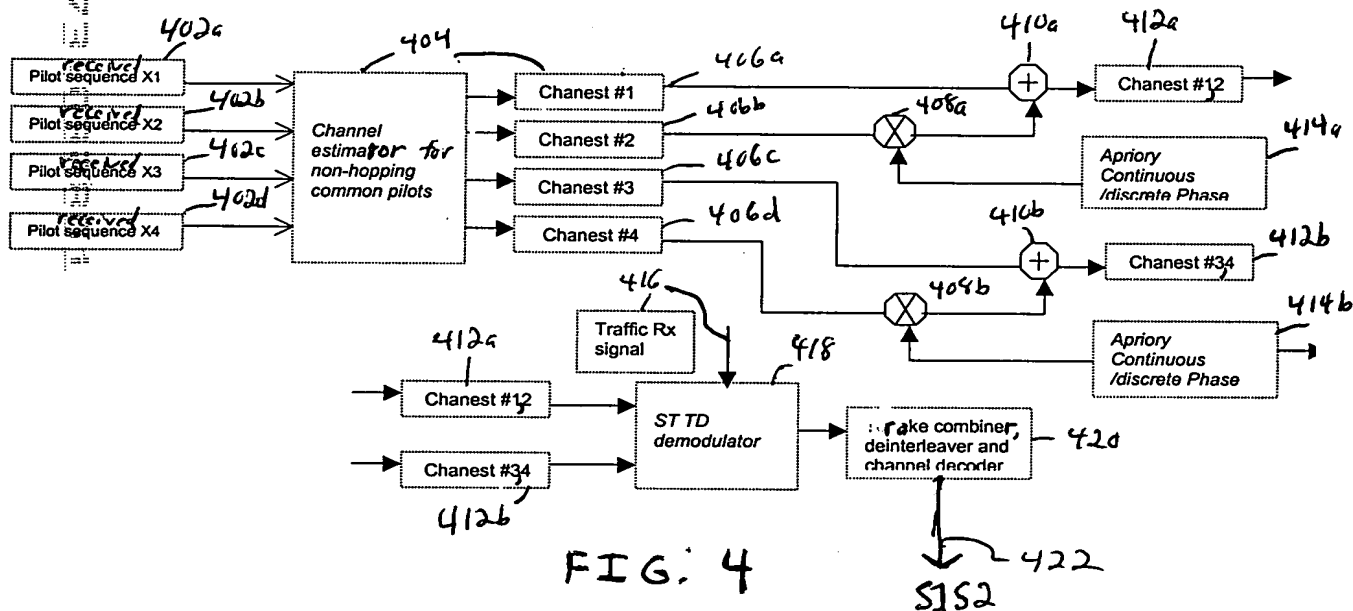


FIG. 4

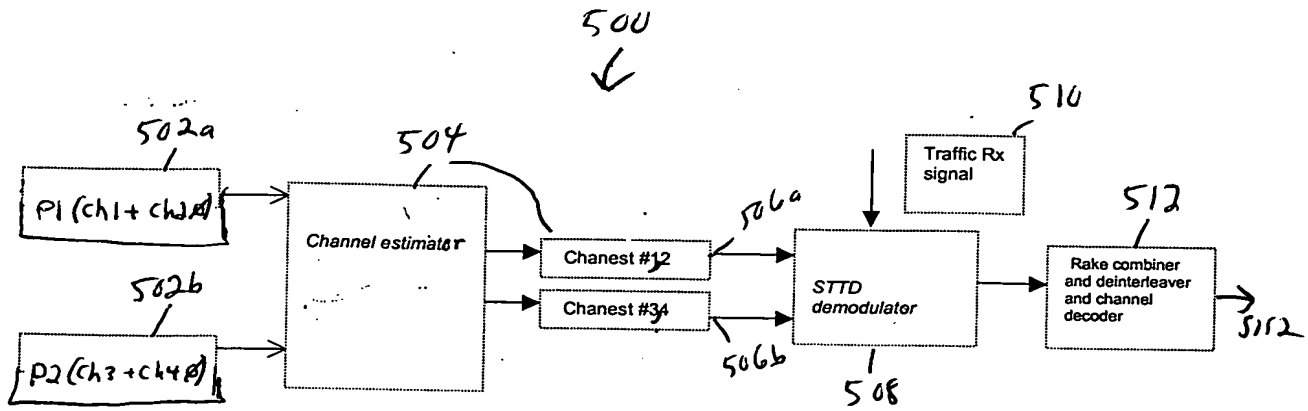


FIG. 5

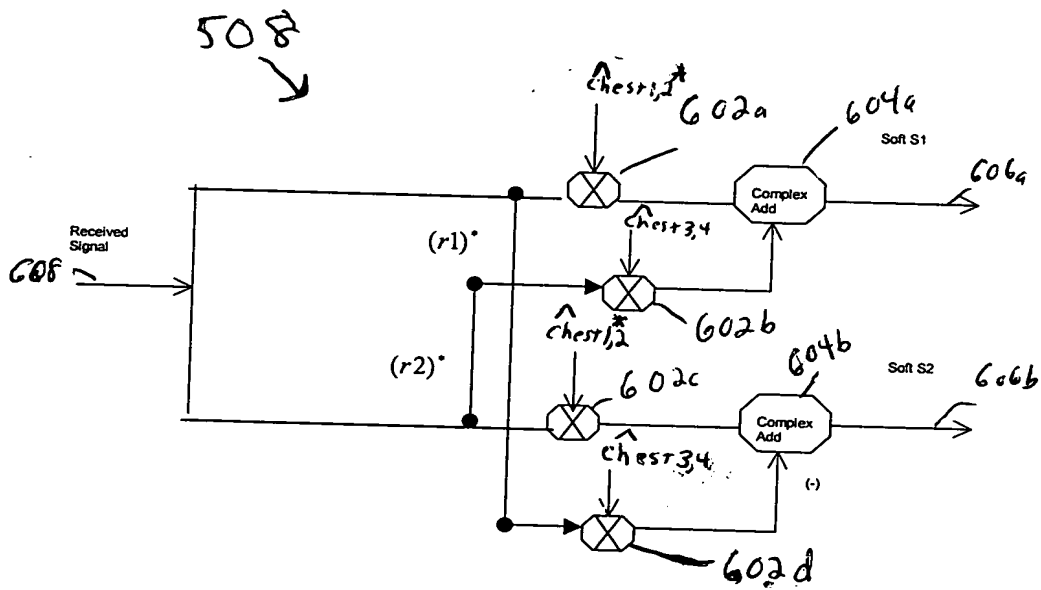


FIG. 6

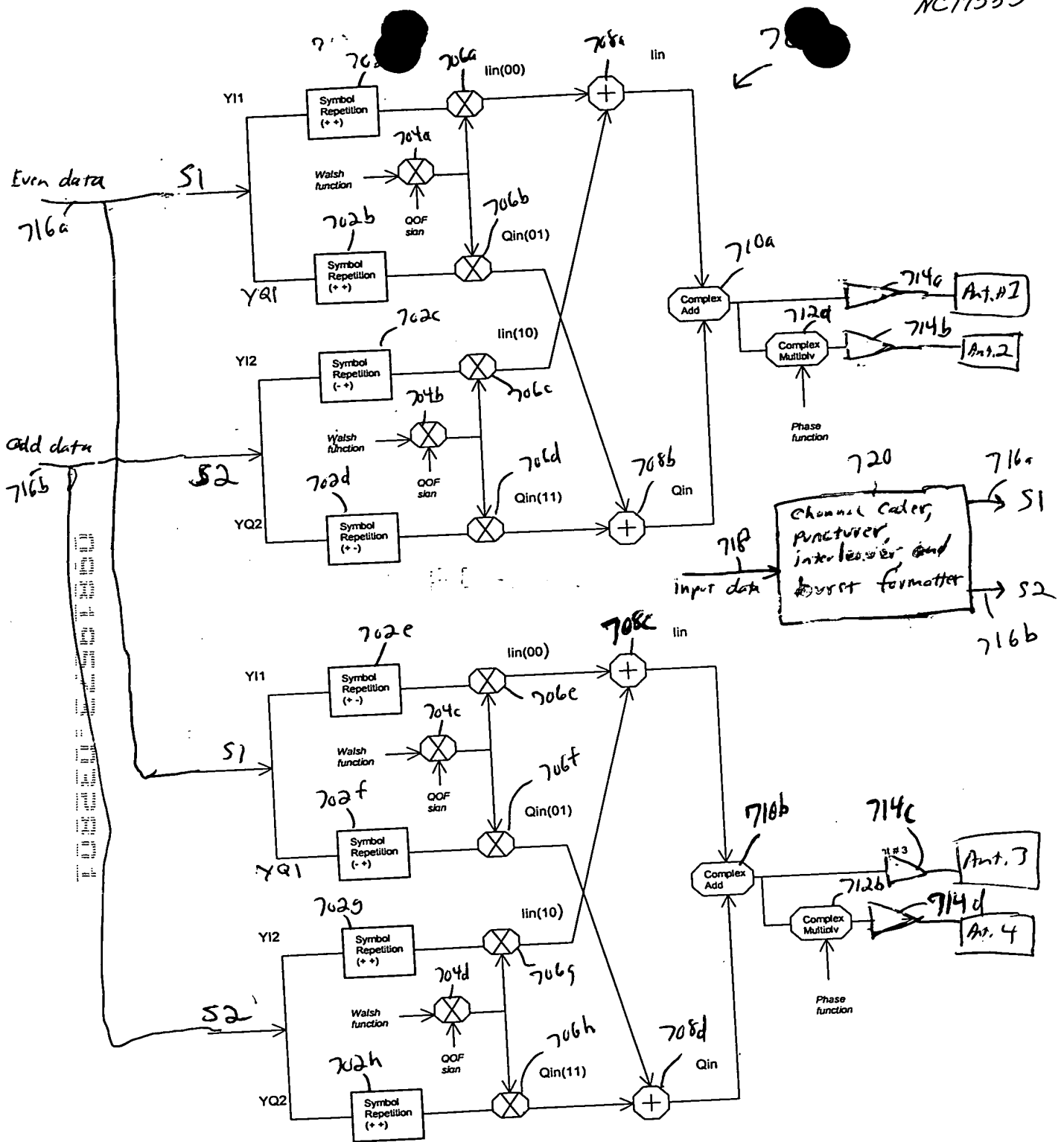


FIG. 7

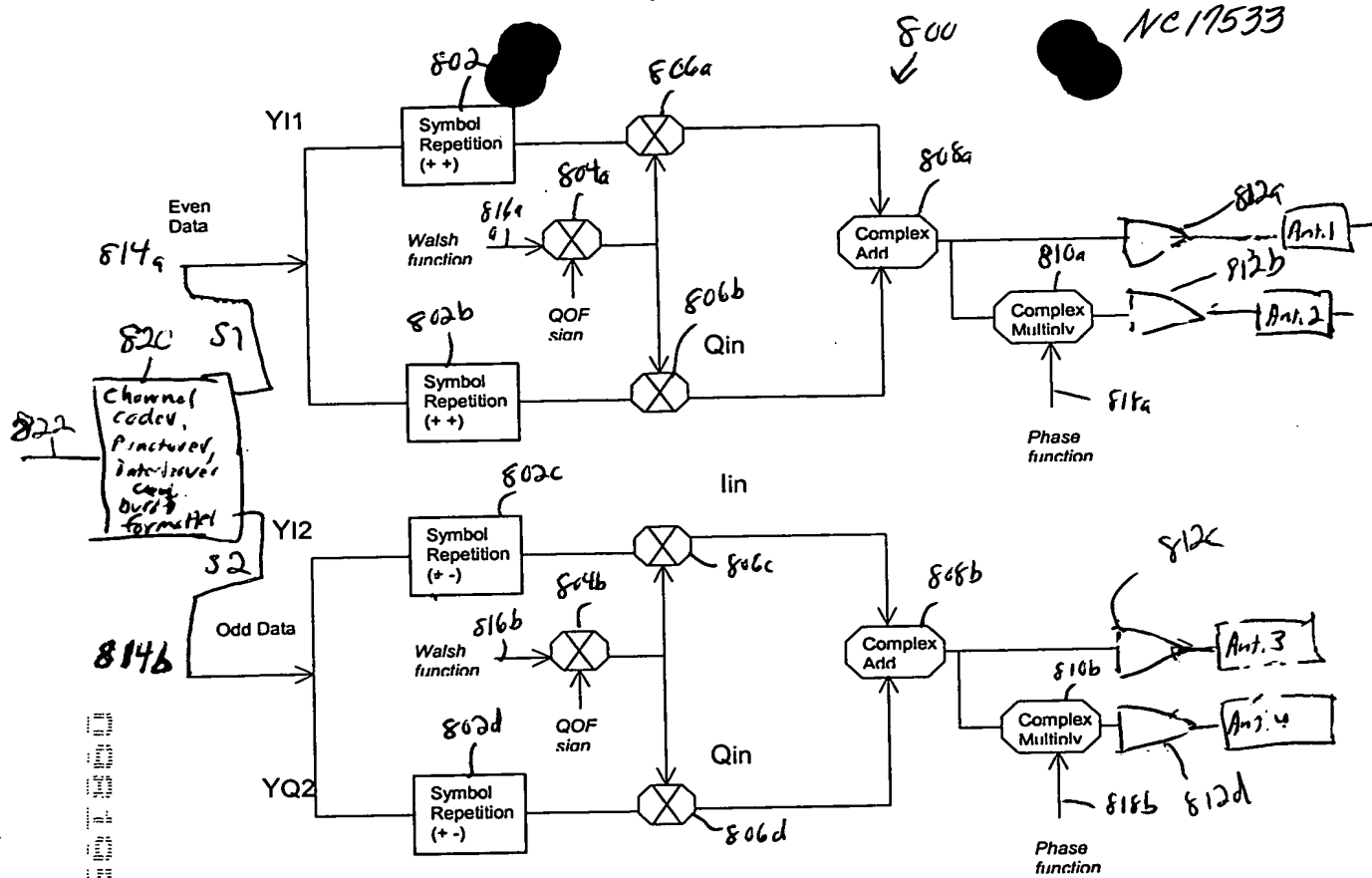


FIG. 8

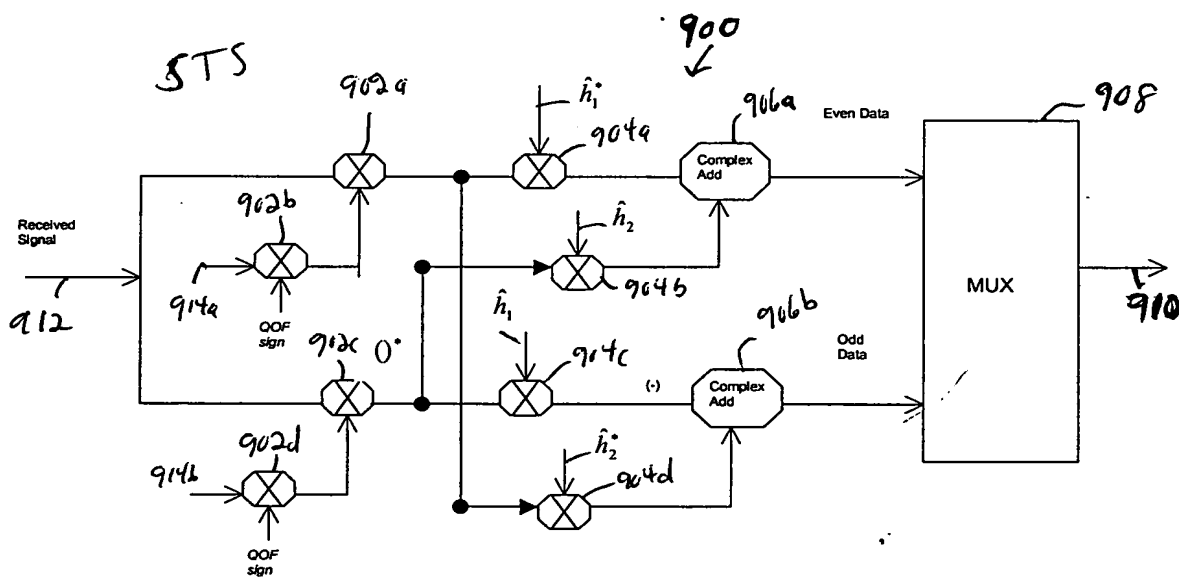


FIG. 9

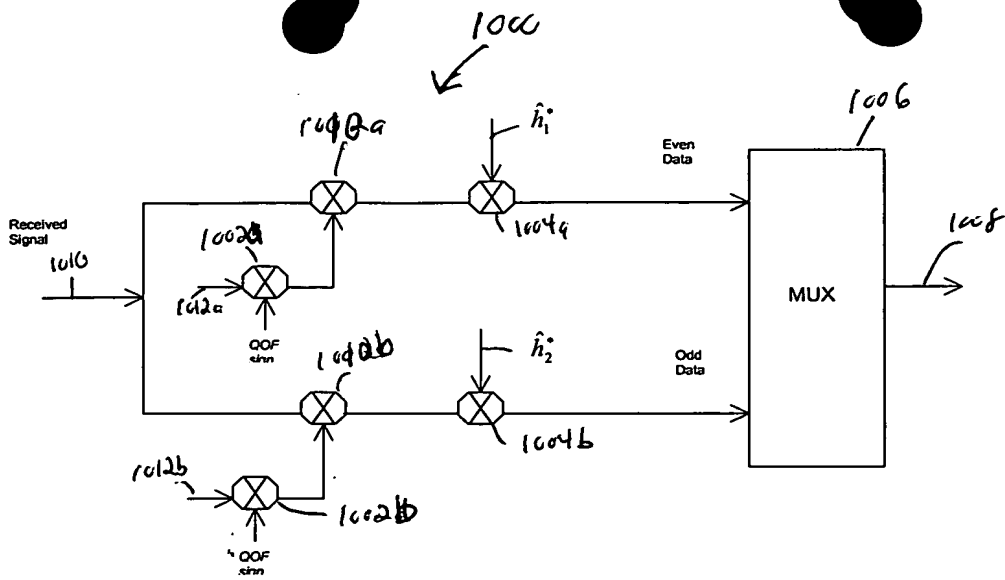


FIG. 10

OTD

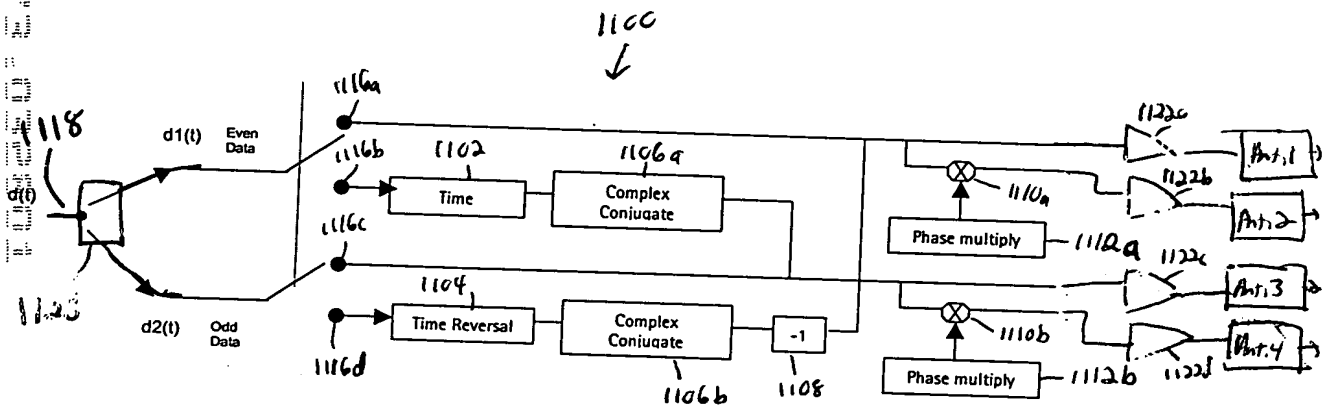


FIG. 11



1200

FIG. 12

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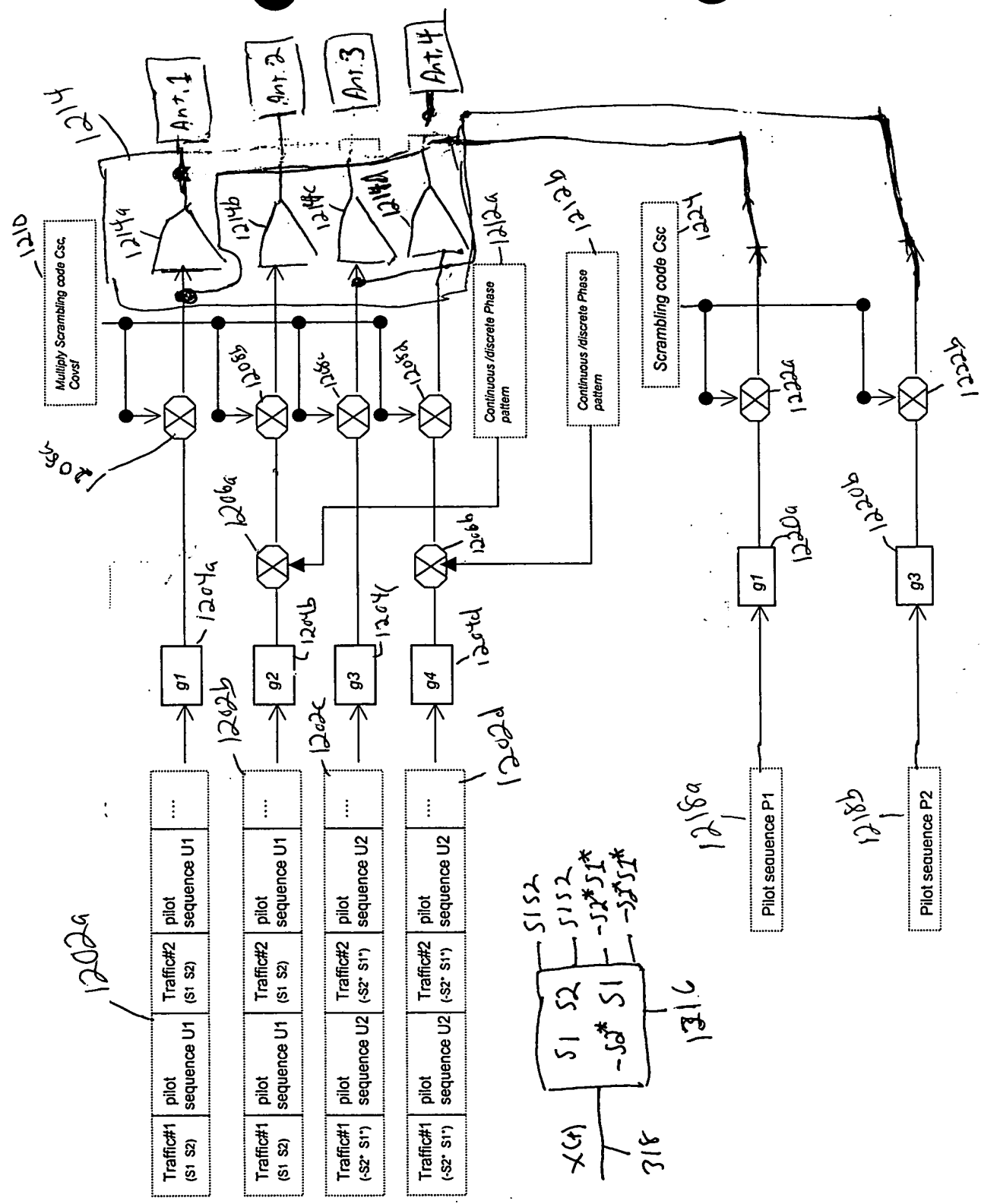


FIG. 12

1300

1304

A priori Continuous /discrete Phase pattern

1302a

Pilot carriers D1

Pilot carriers I11

Pilot carriers D2

Pilot carriers I12

1302d

1308a

Channel #12

Channel #34

1308b

1306

Channel estimator

FIG. 13

1314

deinterleaver and decoder

1310

ST TD demodulator

1312

Received signal

1400

1410a

Channel #12 (t+1)

Phase Shifter

1404a

Channel #1 (t)

Channel #2 (t)

Channel #3 (t)

Channel #4 (t)

1402

Channel estimator

1404b

1404c

1404d

1406a

1406b

+

+

Square

1412a

1412b

Square

1410b

Channel #34 (t+1)

processor

1414

Phase Shifter

1408b

FIG. 14